

Cover Sheet, Block diagram	1-2
Intel LGA775 CPU - Signals	3
Intel LGA775 CPU - Power	4
Intel LGA775 CPU- GND	5
Intel Grantsdale - CPU	6
Intel Grantsdale - Memory	7
Intel Grantsdale - PCI Express	8
Intel Grantsdale - GND	9
ICH6	10-12
Clock Generator - CY28416 & FWH	13
LPC I/O - SMSC 47M997 & KB/MS & COM1 & LPT	14
Azalia CODEC & Interanl SPK	15
ANTI-POP	16
LAN - LAN KINNERITH	17
DDRII DIMM 1 , 2 & Termination & MCH1.8V	18-19
PCI - Express x16 port	20
PCI SLOT 1 & 2 & 3	21
USB Connectors	22
ATX & Front Panel & VGA Connector	23
MS7 ACPI Controller	24
VRM 10 - Intersil HIP 6566 3 phase	25
FAN Controller & IDE & SATA	26
VIA VT-6307 IEEE1394 Controller	27
Manual Parts	28
GPIO & JUMPER SETTING	29
POWER MAP	30
Revision History	31

MS-7174H1

Version 100

Intel (R) Grantsdale (GMCH) + ICH6 Chipset
Intel Prescott LGA775 Processor

CPU:

Intel Prescott Celeron D 350J (3.2GHz), P4 550J (3.4GHz)

System Chipset:

**Intel Grantsdale - GMCH (North Bridge 915GV or 910GE)
Intel ICH6 (South Bridge)**

On Board Chipset:

**BIOS -- FWH FLASH 4Mb
AC97 AUDIO -- ALC880
LPC Super I/O -- SMSC47M997
LAN -- Intel 82562GT
1394 -- VIA VT-6307
CLOCK -- Cypress CY28416**

Main Memory:

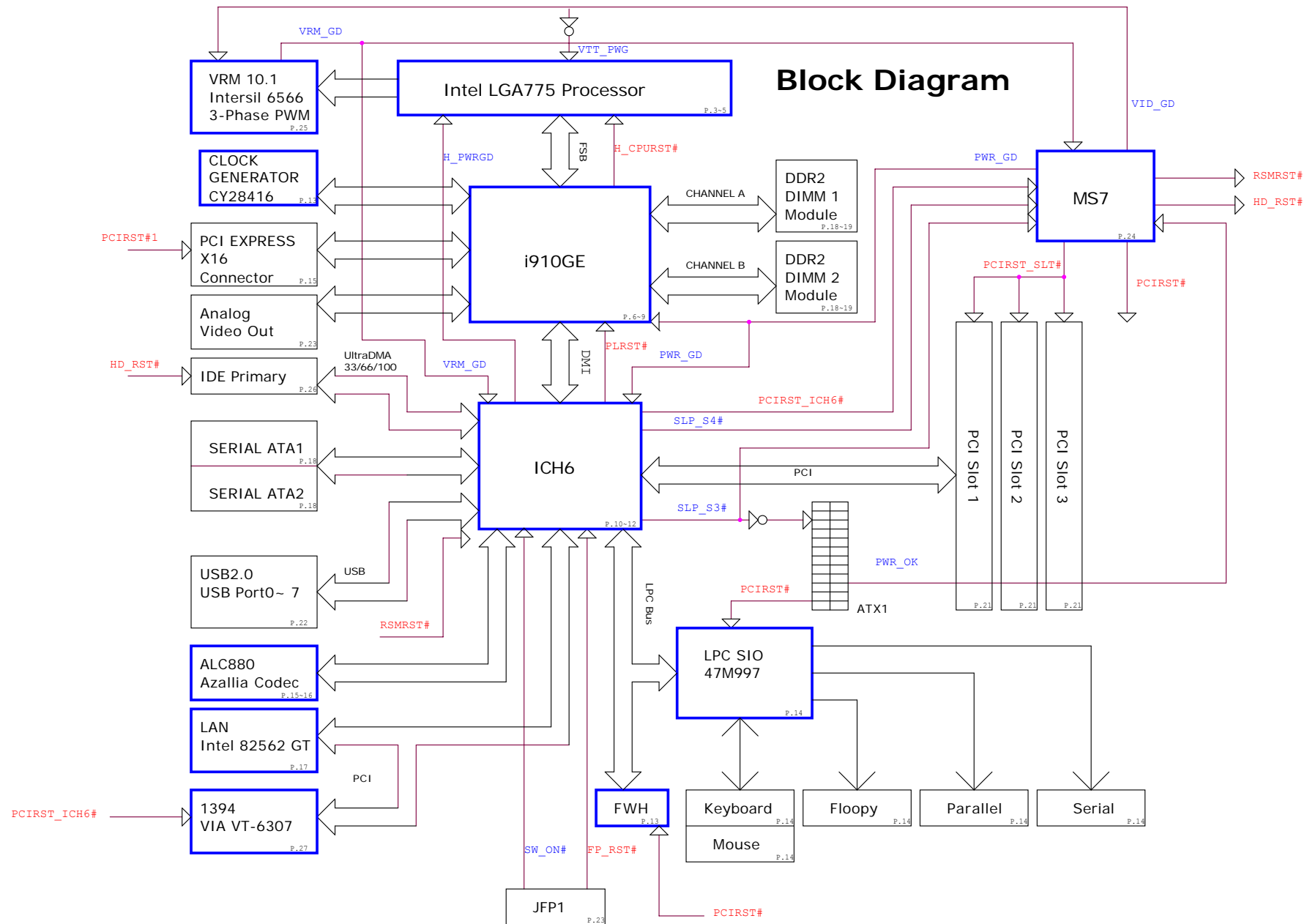
2 CHANNEL DDR II * 1 (Max 2GB)

Expansion Slots:

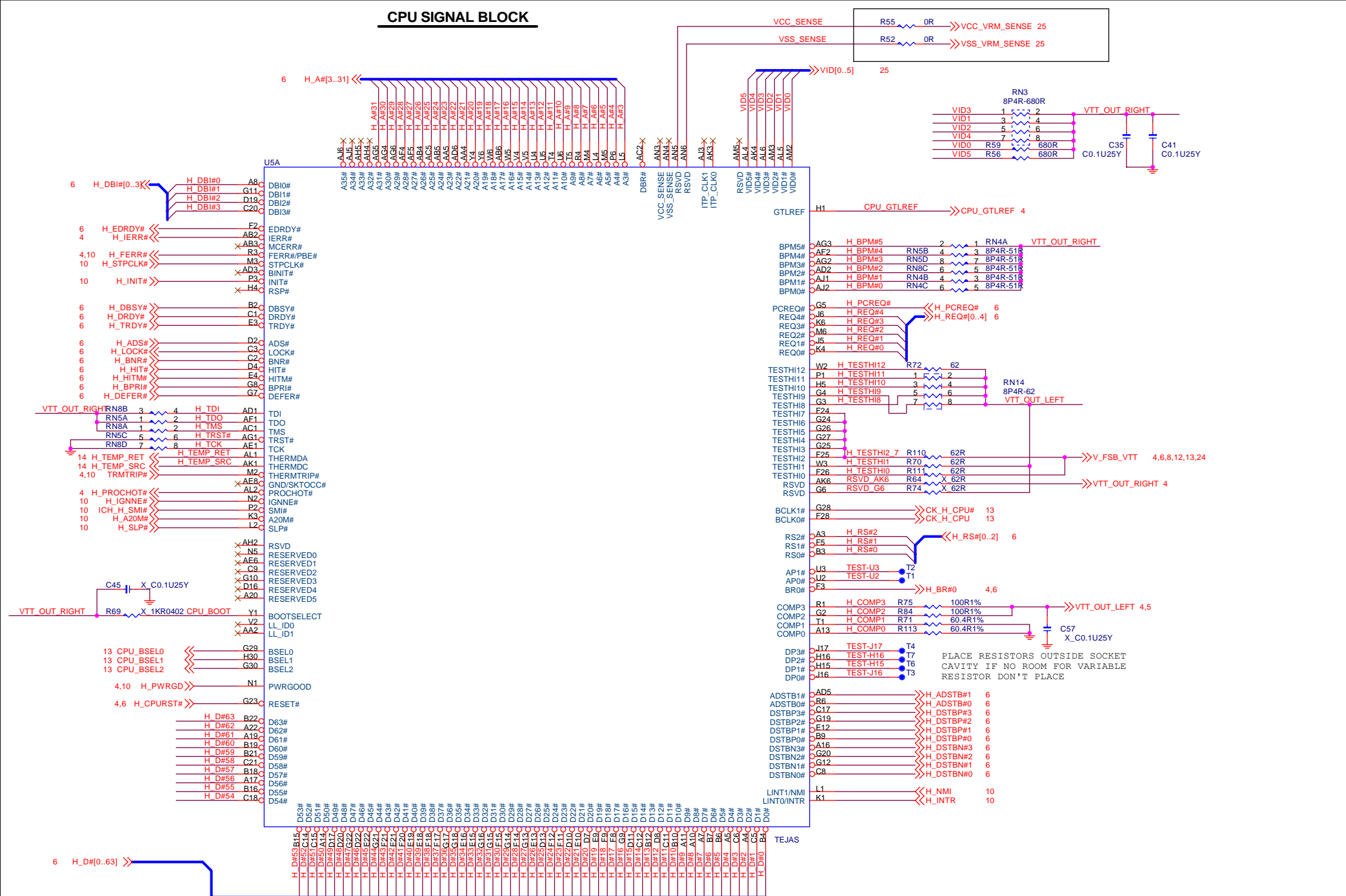
PCI 2.3 SLOT * 3

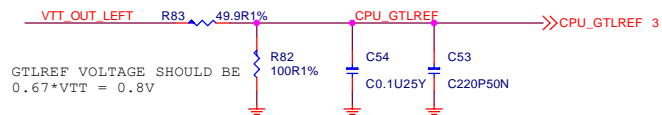
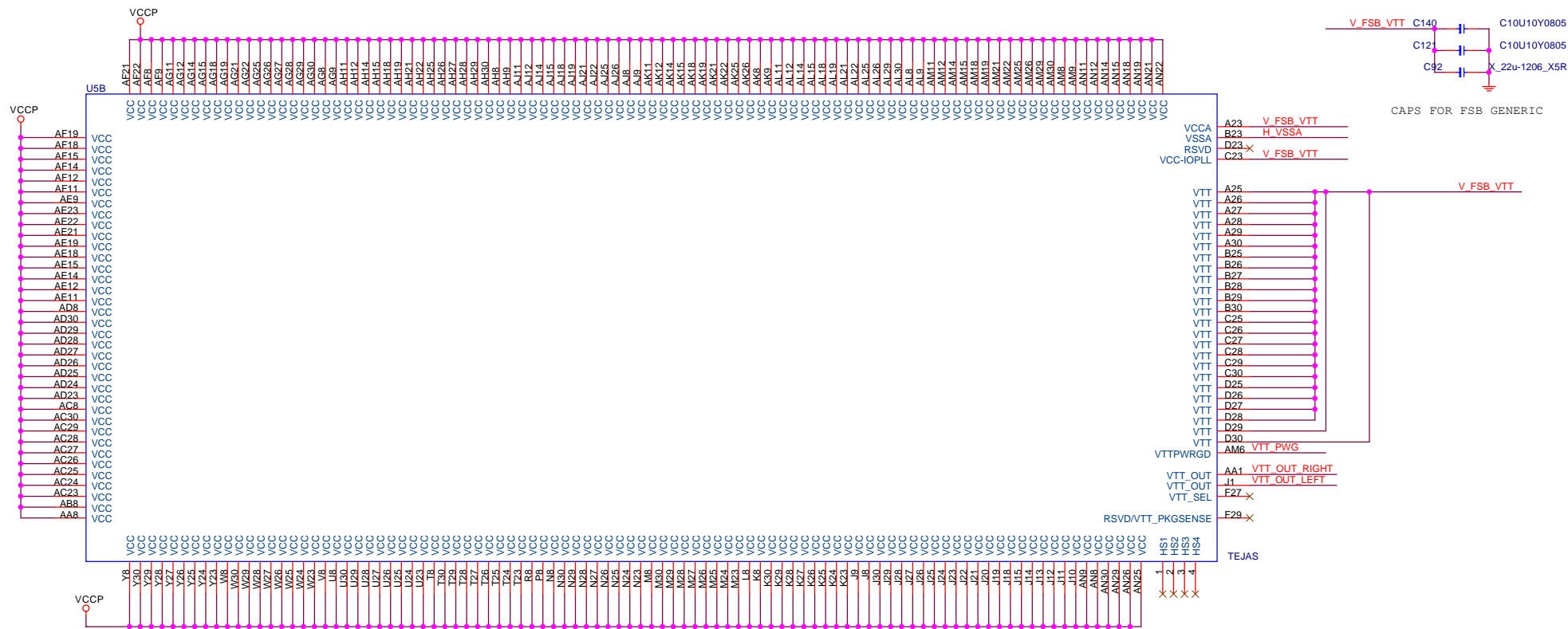
Intersil PWM:

Controller: INTERSIL 6566 3PHASE

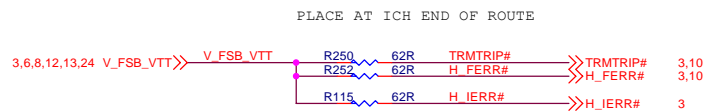
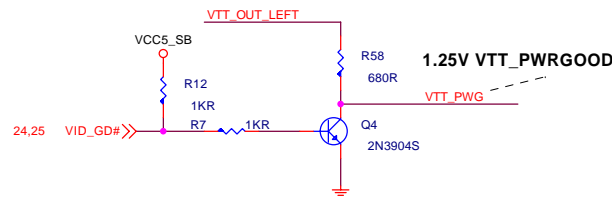
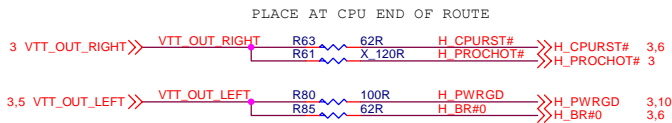
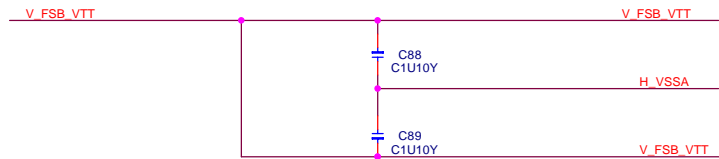


CPU SIGNAL BLOCK

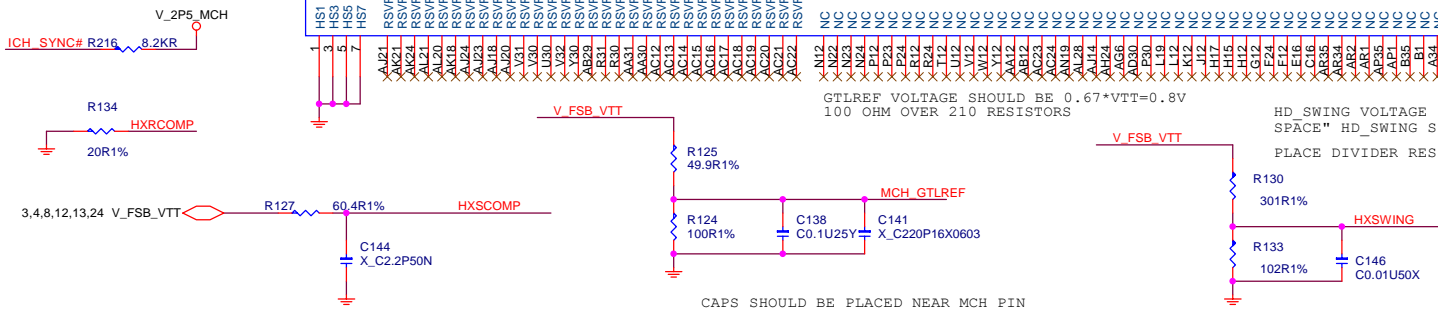
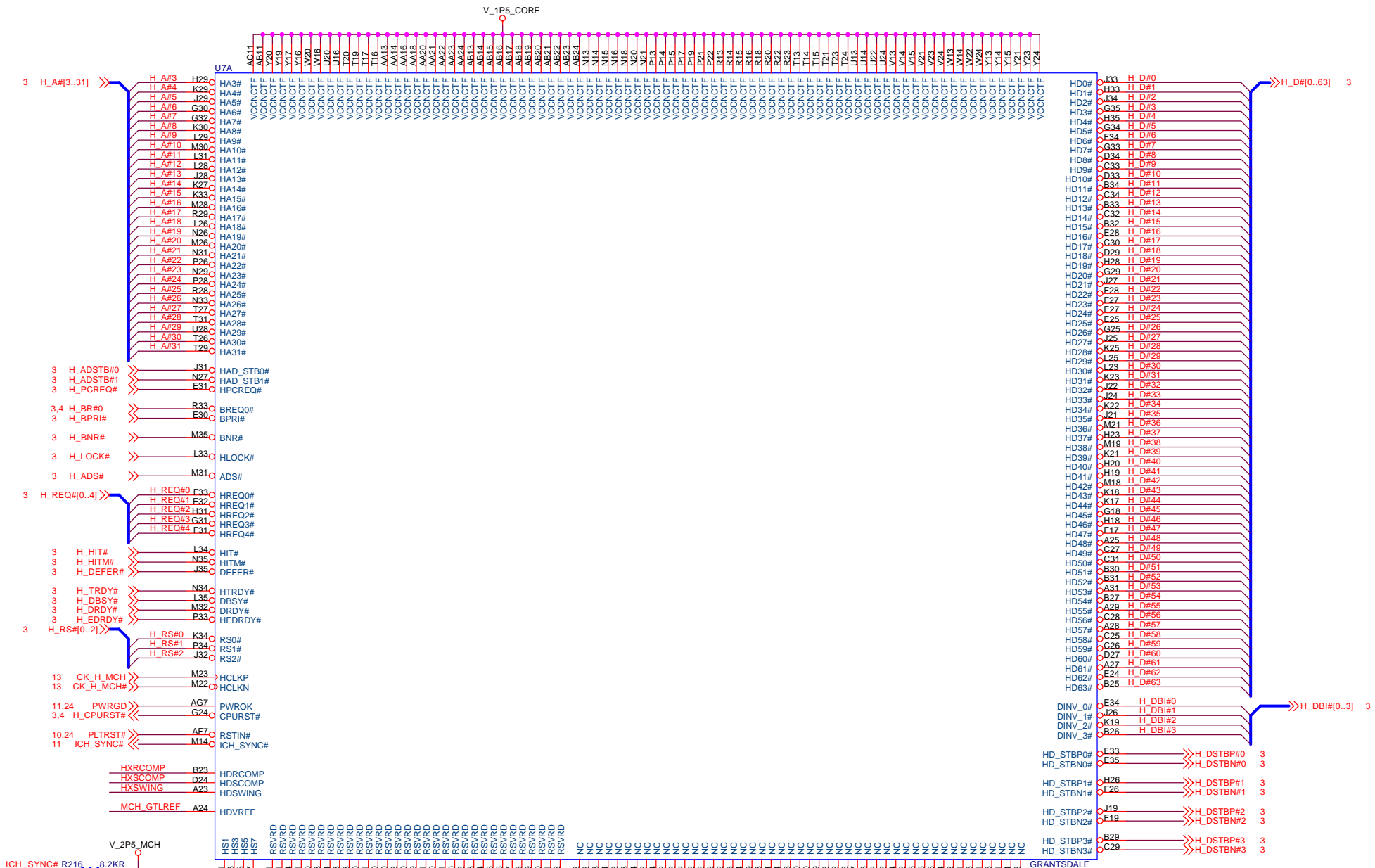




PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
TRACE WIDTH TO CAPS MUST BE SMALLER THAN 12MILS

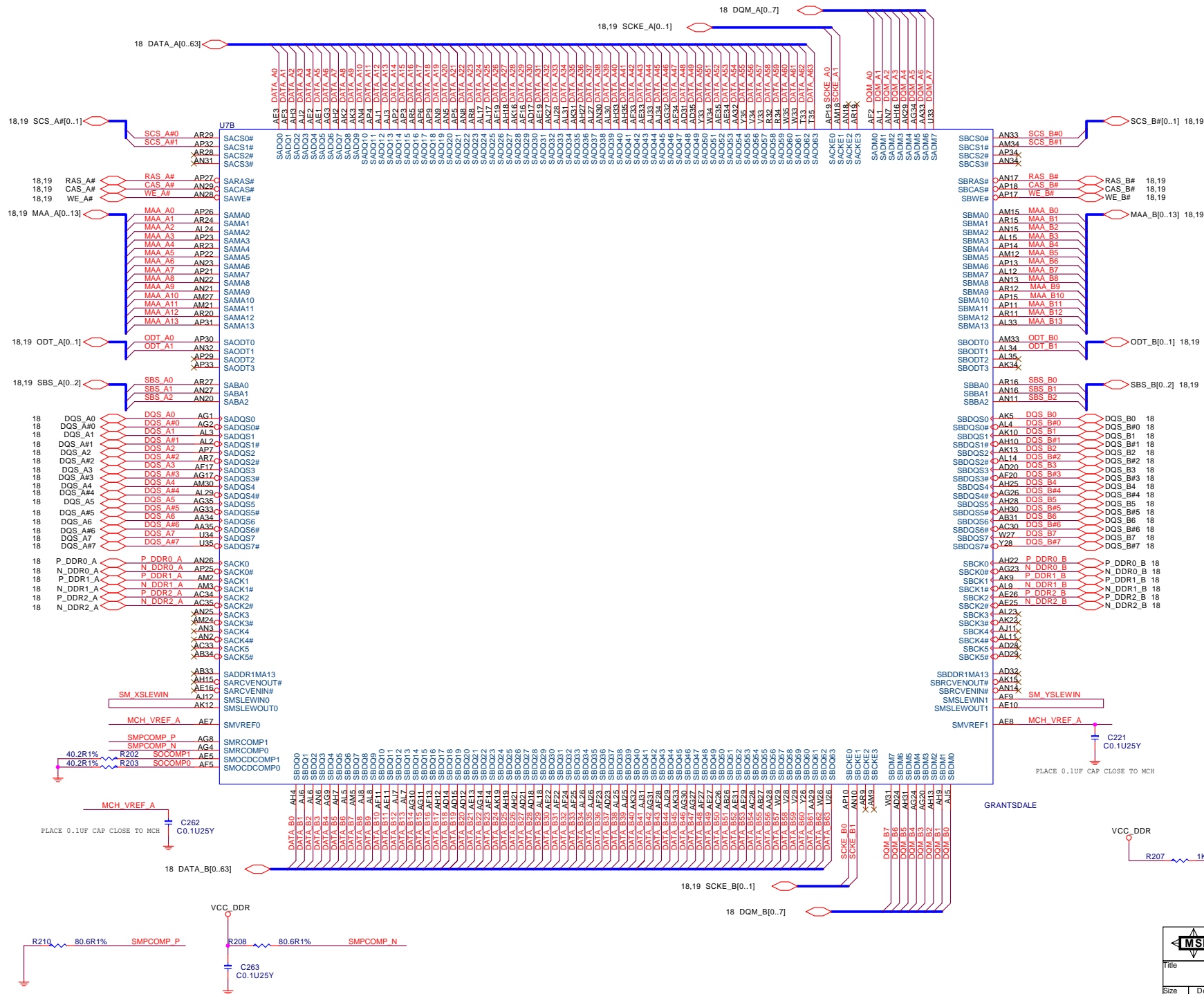


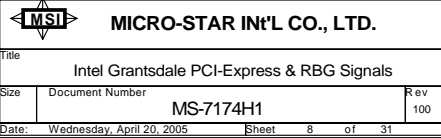
MSI MICRO-STAR INT'L CO., LTD.			
Title Intel LGA775 CPU - Power			
Size	Document Number		Rev
	MS-7174H1		100
Date:	Wednesday, April 20, 2005	Sheet	4 of 31

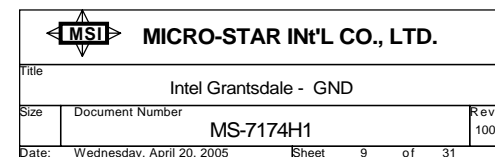


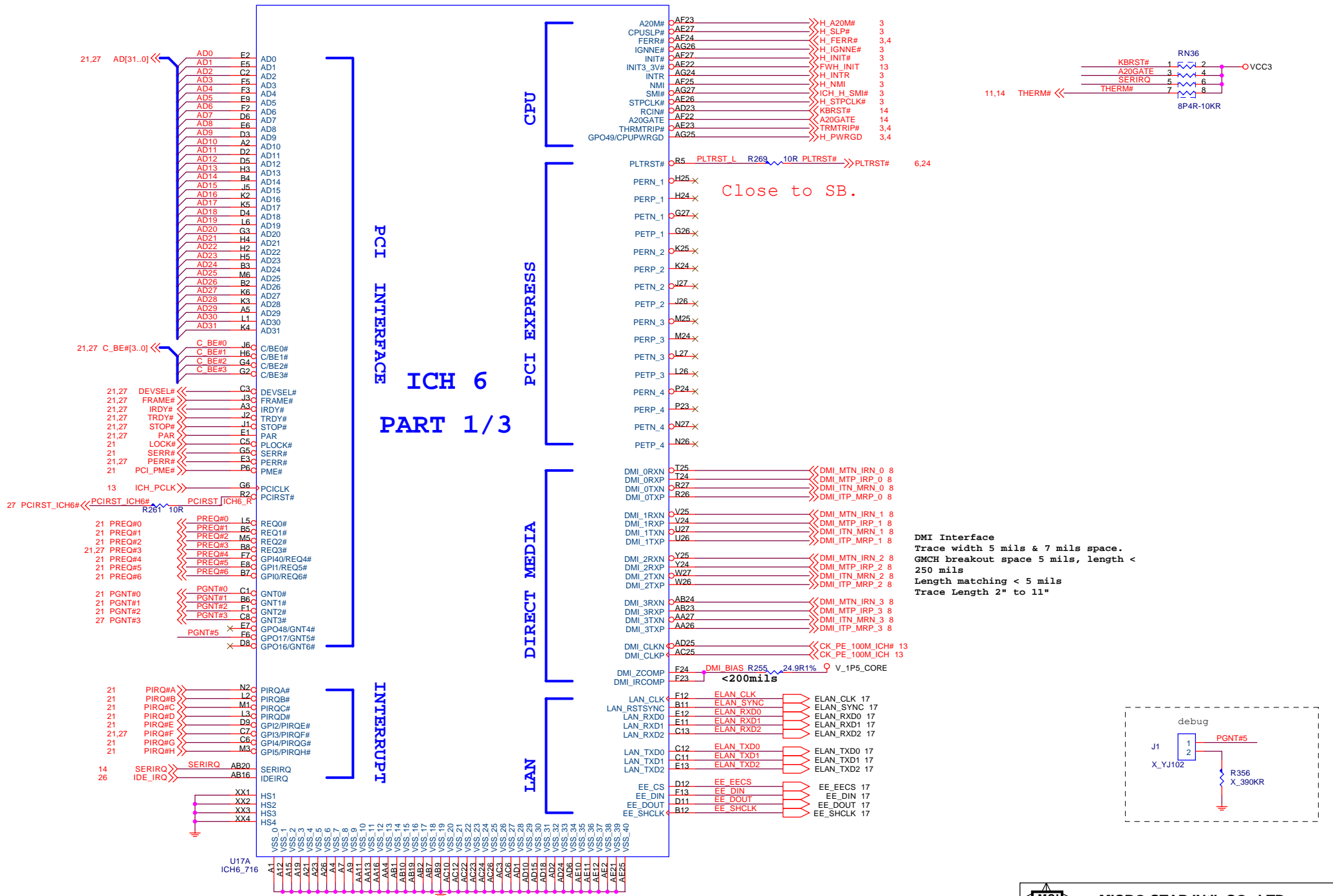
GTLREF VOLTAGE SHOULD BE $0.67 \cdot V_{TT} = 0.8V$
100 OHM OVER 210 RESISTORS

HD SWING VOLTAGE "10 MIL TRACE , 7 MIL SPACE" HD_SWING S/B $1/3 \cdot V_{TT} \pm 2\%$
PLACE DIVIDER RESISTOR NEAR VTT

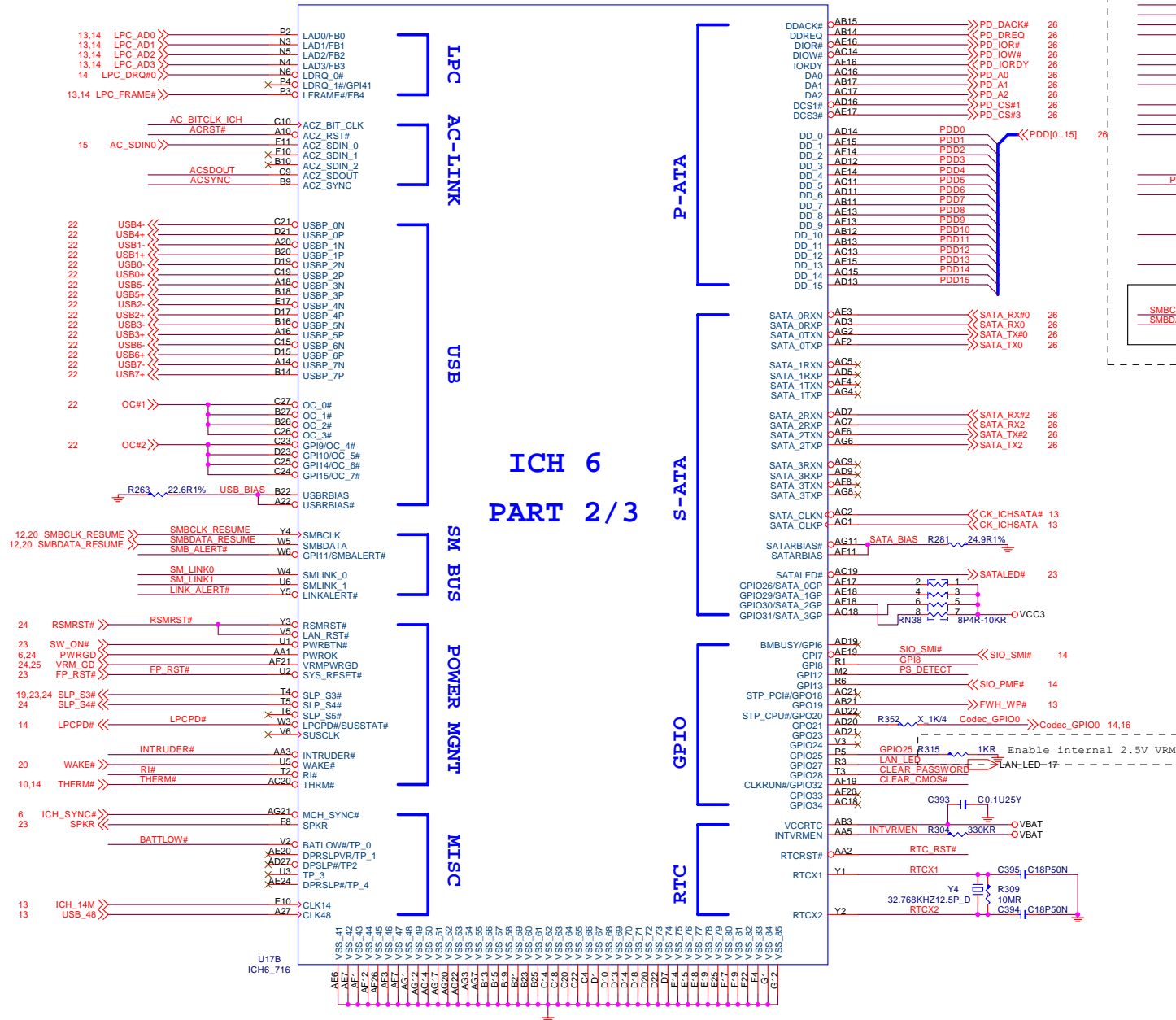






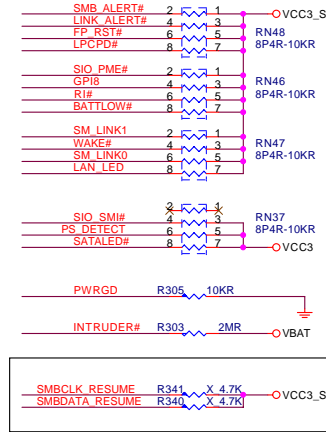


ICH 6 PART 2/3

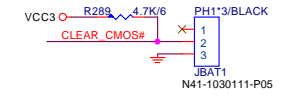


ICH6 STRAPPING RESISTORS

ALL COMPONENTS CLOSE TO ICH6
Trace length is less than 3inches to ICH6.

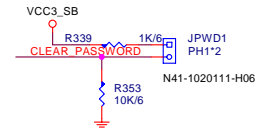


CLEAR CMOS JUMPER



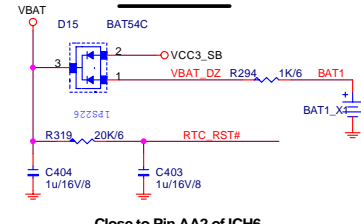
CMOS CLEAR	NORMAL	CLEAR
JBAT1	(1-2)	(2-3)

PASSWORD CLEAR JUMPER



JPWD1	Short	Normal
OPEN	CLEAR	PASSWORD

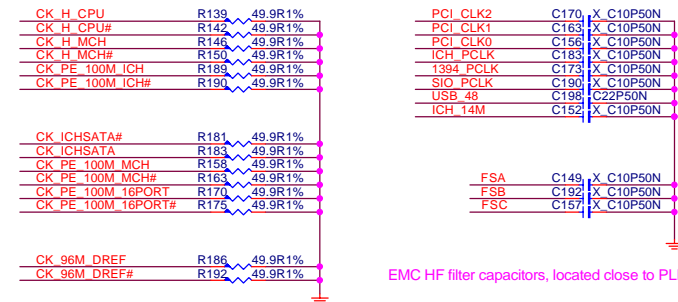
BATTERY



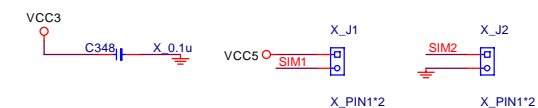
Close to Pin AA2 of ICH6.



Trace length less than 0.5inches



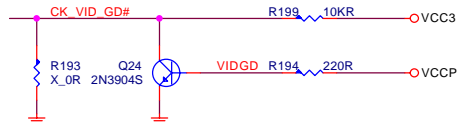
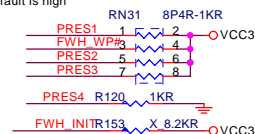
EMC HF filter capacitors, located close to PLL



If you place the jumper very closed to FWH bios socket, please use the same clock with FWH. But if you can not place it so close, please use another clock to support it.

FWH Resistors

default is high



Title					CY28416 & FWH				
Size	Document Number							Rev	
	MS-7174H1							100	
Date:	Wednesday, April 20, 2005			Sheet	13	of	31		

Pin connection diagram for the ADXL345 I2C interface. The diagram shows the ADXL345 chip with pins 1 through 8. Pin 1 is connected to GND. Pin 2 is connected to VCC3. Pin 3 is connected to SIO_ADDR. Pin 4 is connected to VCC3. Pin 5 is connected to SIO_ADDR. Pin 6 is connected to VCC3. Pin 7 is connected to SIO_ADDR. Pin 8 is connected to VCC3. The SIO_ADDR pin is also connected to a pull-up resistor R20 (4.7K/6) to VCC3. The VCC3 pin is also connected to a pull-up resistor R21 (4.7K/6) to VCC3. The GND pin is connected to a pull-up resistor R22 (4.7K/6) to GND. The diagram also shows the pin connections for the ADXL345 chip: Pin 1 is connected to GND. Pin 2 is connected to VCC3. Pin 3 is connected to SIO_ADDR. Pin 4 is connected to VCC3. Pin 5 is connected to SIO_ADDR. Pin 6 is connected to VCC3. Pin 7 is connected to SIO_ADDR. Pin 8 is connected to VCC3. The SIO_ADDR pin is also connected to a pull-up resistor R20 (4.7K/6) to VCC3. The VCC3 pin is also connected to a pull-up resistor R21 (4.7K/6) to VCC3. The GND pin is connected to a pull-up resistor R22 (4.7K/6) to GND.

SIO_ADDR
H: 0x04E
L: 0x02E (DEFAULT)

	ID3	ID2	ID1	ID0
Gypsum:	0	0	0	1
Graphite:	0	0	1	0

PARALLEL PORT

The figure illustrates the pin connections for a parallel port interface. It includes three sub-diagrams showing the connection of various pins to the 80486 and the 8255 PPI. The pins are labeled with their respective functions and pin numbers. The connections are as follows:

- Left Diagram:**
 - VCCs (D3) to 1N4148 SOD123 LPT VC
 - SLIN# R 2 to 1 SLIN# 1 2
 - PRND3 R 4 to 3 PRND3 3 4
 - PINIT# R 6 to 5 PINIT# 5 6
 - PRND2 R 8 to 7 PRND2 7 8
 - PRND7 R 2 to 1 PRND7 1 2
 - PRND6 R 4 to 3 PRND6 3 4
 - PRND5 R 6 to 5 PRND5 5 6
 - PRND4 R 8 to 7 PRND4 7 8
 - SLCT R 2 to 1 SLCT 1 2
 - PE R 4 to 3 PE 3 4
 - BUSY R 6 to 5 BUSY 5 6
 - ACK# R 8 to 7 ACK# 7 8
 - ERR# R 8 to 7 ERR# 7 8
 - PRND1 R 6 to 5 PRND1 5 6
 - AFD# R 4 to 3 AFD# 3 4
 - PRND0 R 2 to 1 PRND0 1 2
 - RSTB# R 86 to 33R RSTB# R87 2.2KR
- Middle Diagram:**
 - PRND2 1 to 2
 - PINIT# 3 to 4
 - PRND3 5 to 6
 - SLIN# 7 to 8
 - PRND4 1 to 2
 - PRND5 3 to 4
 - PRND6 5 to 6
 - PRND7 7 to 8
 - ACK# 1 to 2
 - BUSY 3 to 4
 - PE 5 to 6
 - SLCT 7 to 8
 - PRND0 7 to 8
 - AFD# 5 to 6
 - PRND1 3 to 4
 - ERR# 1 to 2
 - RSTB#
- Right Diagram:**
 - RSTB# 1 to 14
 - PRND0 2 to 15
 - PRND1 3 to 16
 - PRND2 4 to 17
 - PRND3 5 to 18
 - PRND5 7 to 20
 - PRND6 8 to 21
 - PRND7 9 to 22
 - ACK# 10 to 23
 - BUSY 11 to 24
 - PE 12 to 25
 - SLCT 13 to 26
 - AFD#
 - PINIT#
 - LPT SLIN#
 - CONN LPT
 - KBGND
 - CP2
 - CP1
 - CP12
 - KBGND
 - LPT SLIN# FB7
 - SLIN#
 - 120S/0603

[illegible]

FDD1

1 2 DRVDDEN#

3 4 INDEX#

5 6 MOA#

7 8 DSA#

9 10

11 12

13 14

15 16 DIR#

17 18 STEP#

19 20

21 22 WRDATA#

23 24 WE#

25 26 TRACK0#

27 28 WP#

29 30 RRDATA#

31 32 HEAD#

33 34 DSKCHG#

FLOPPY

AUX IN

JCD1
CD1*4/BLACK

CD IN

RET_AUX_L R286 4.7K/4

LINE1_L

LINE1_R

RET_AUX_R R312 4.7K/4

LINE2_L

LINE2_R

MIC2_L

MIC2_R

CDL C366 2 1 1u/10V/6

CDGND C356 2 1 1u/10V/6

CDR C365 2 1 1u/10V/6

SENSE_A

LINE2_L

LINE2_R

MIC1_IN_R C387 1u/16V/8

MIC1_IN_L C375 1u/16V/8

MIC1_R C360 1u/16V/8

MIC1_L C361 1u/16V/8

MIC1_VREFO_L R288 4.7K/4

MIC1_VREFO_R R287 4.7K/4

R299 22K/4

R302 22K/4

RET_AUX_R

RET_AUX_L

MIC1_R

MIC1_L

0.1u/25V/6

[illegible]

The schematic diagram is divided into two main sections: "Standby POP noise" and "SPDIF IN & OUT".

Standby POP noise section: This section shows the power supply and signal input for the SOT233SGD component. It includes a VCC3_SB supply connected through a 10K/4 resistor (R290) to the VCC pin of the SOT233SGD. A 12V supply is connected through a 560K/6 resistor (R293) to the GND pin. A 5V_R supply is connected through a 220K/4 resistor (R322) to the SOT233SGD. A 1K/4 resistor (R295) is connected to the AC_RST# signal. A 2N3904S transistor (Q35) is connected to the SOT233SGD. A 4.7u/10V/8 capacitor (C389) is connected to the GND pin. A 10K/4 resistor (R298) is connected to the LINE1_1R signal.

SPDIF IN & OUT section: This section shows the SPDIF input and output signals. The SPDIF_IN signal is connected through a 10K/4 resistor (R320) to the JACK-RCA3P_black_3 input. A 10K/4 resistor (R316) is connected to the GND pin. A 0.01u50X capacitor (C33) is connected to the SPDIF_IN signal. A 100P50N capacitor (C34) is connected to the GND pin. The SPDIF_OUT signal is connected through a 200R resistor (R48) to the JACK-RCA3P_yellow_3 input. A 100R resistor (R49) is connected to the GND pin. A 0.01u50X capacitor (C32) is connected to the SPDIF_OUT signal. A 100P50N capacitor (C31) is connected to the GND pin.

Rear audio jack

CONNECTOR

ALC880 JACK

AUDIO1

AUDIO_JACK6

LINE1 JD

FRONT JD

MIC1 JD

CEN JD

SURR JD

SURRBACK JD

LINE1 1R

LINE1 1L

LINE FOUTR

LINE FOUTL

MIC1 R

MIC1 L

LFE OUT

CENTER OUT

SURR_OUTR

SURR_OUTL

SURRBACK R

SURRBACK L

LINE-IN3

LINE-IN4

LINE-IN5

LINE-IN2

LINE-OUT3

LINE-OUT4

LINE-OUT5

LINE-OUT2

MIC3

MIC4

MIC5

MIC2

CENTER3

CENTER4

CENTER5

CENTER2

SURROUND3

SURROUND4

SURROUND5

SURROUND2

SURROUND-SIDE3

SURROUND-SIDE4

SURROUND-SIDE5

SURROUND-SIDE2

C219

C218

C255

C254

C213

C214

C217

C256

C215

C216

C211

C212

X_100p/50V/6

R5

L5

G3

G4

G5


G6

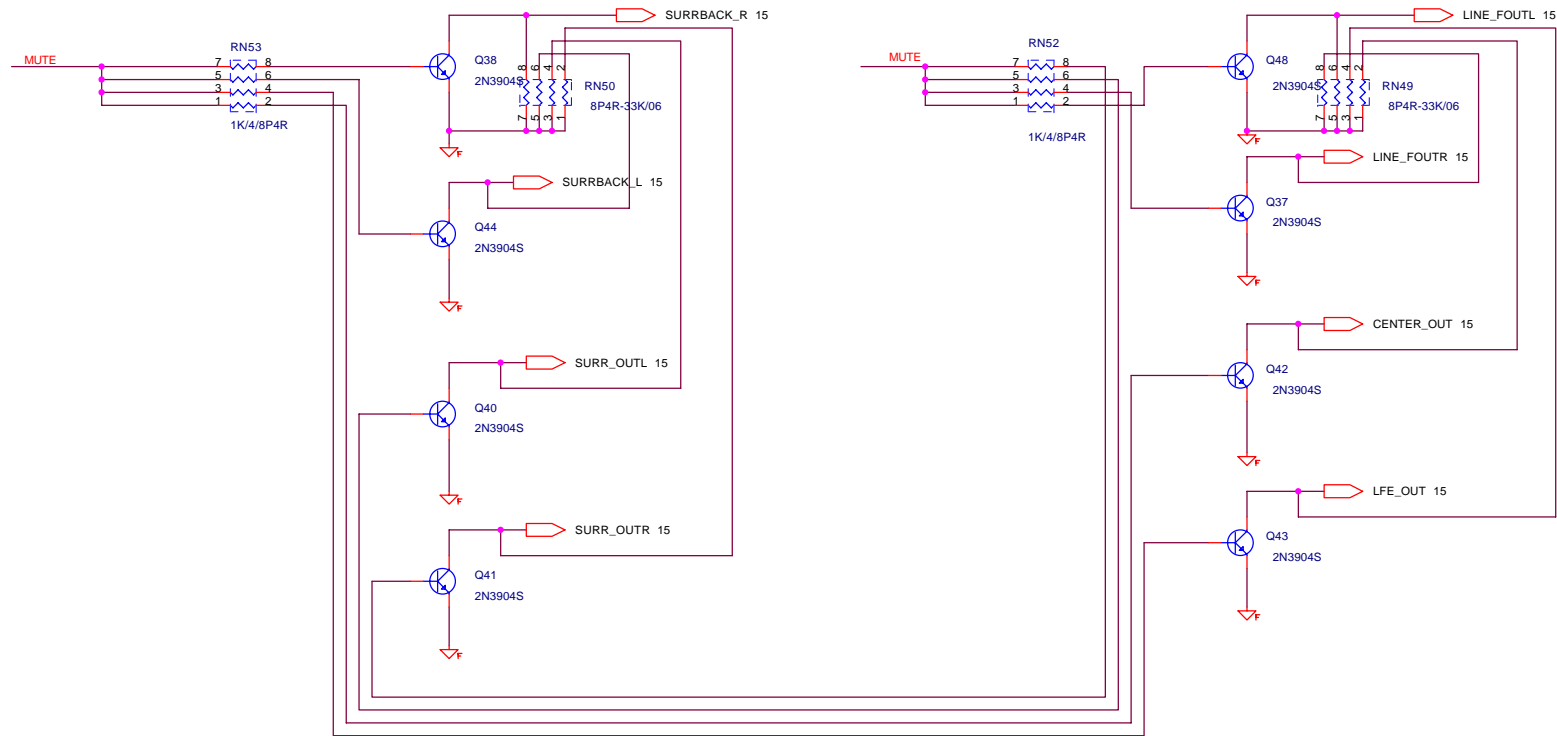
ORANGE

BLACK

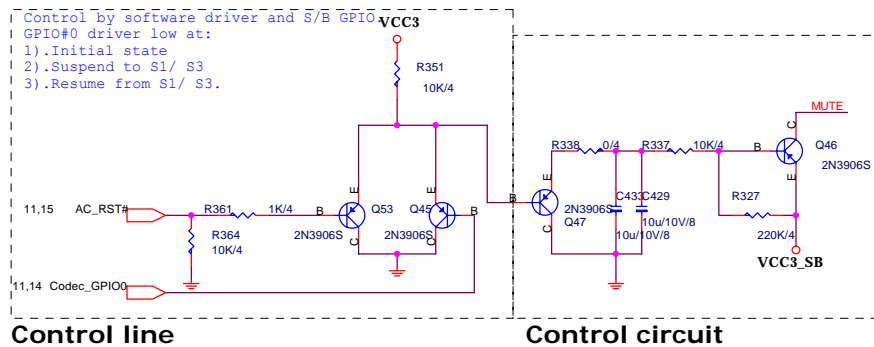
GRAY

ALC880 JACK DETECT			
SENSE_A	R284	5.1K/4/1	FRONT_JD
	R285	10K/4/1	LINET_JD
	R282	20K/4/1	MIC1_JD
	R286	39.2K/4/1	SURR_JD
SENSE_B	R318	5.1K/4/1	SURRBACK_JD
	R317	10K/4/1	CEN_JD
	R362	X_0R	AZ_FRONT_JD

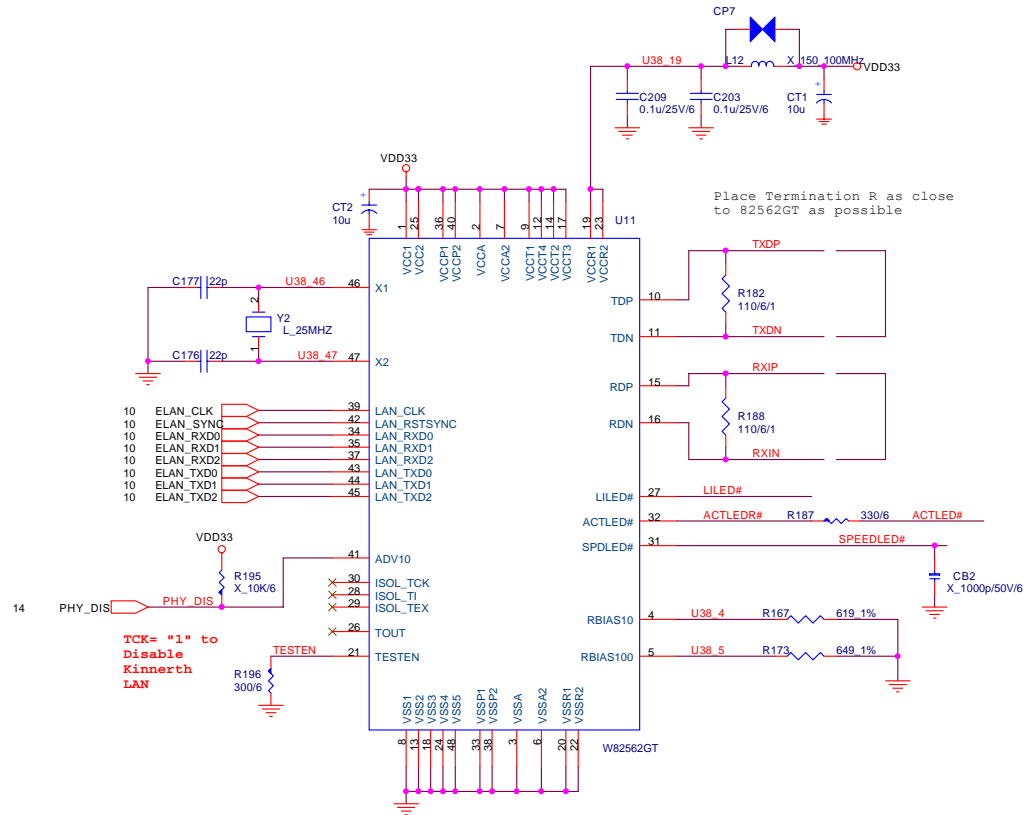
 MICRO-STAR INT'L CO., LTD.	
Title	
Azalia & Interanl SPK	
Size	Document Number
	MS-7174H1
Date	Wednesday April 20 2005
Sheet	15 of 31
Rev	100



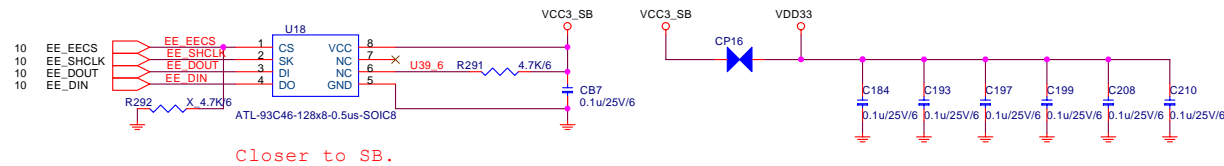
darlington circuit



LAN - KINNERITH

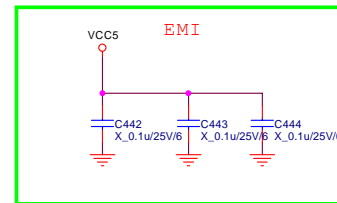
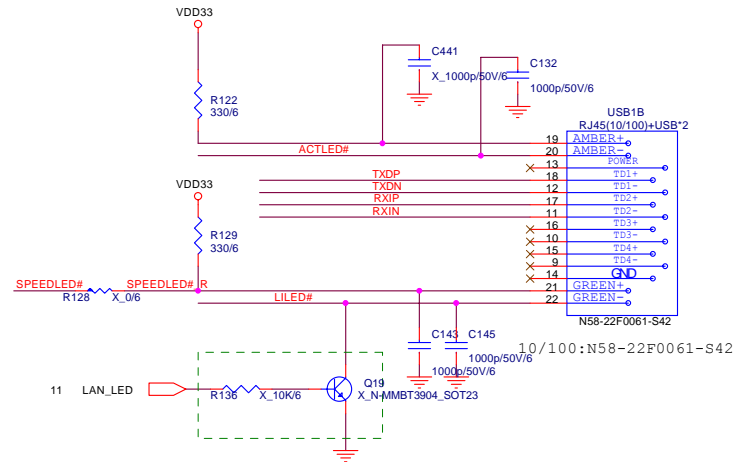


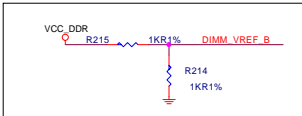
EEPROM

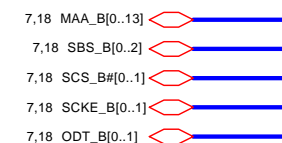
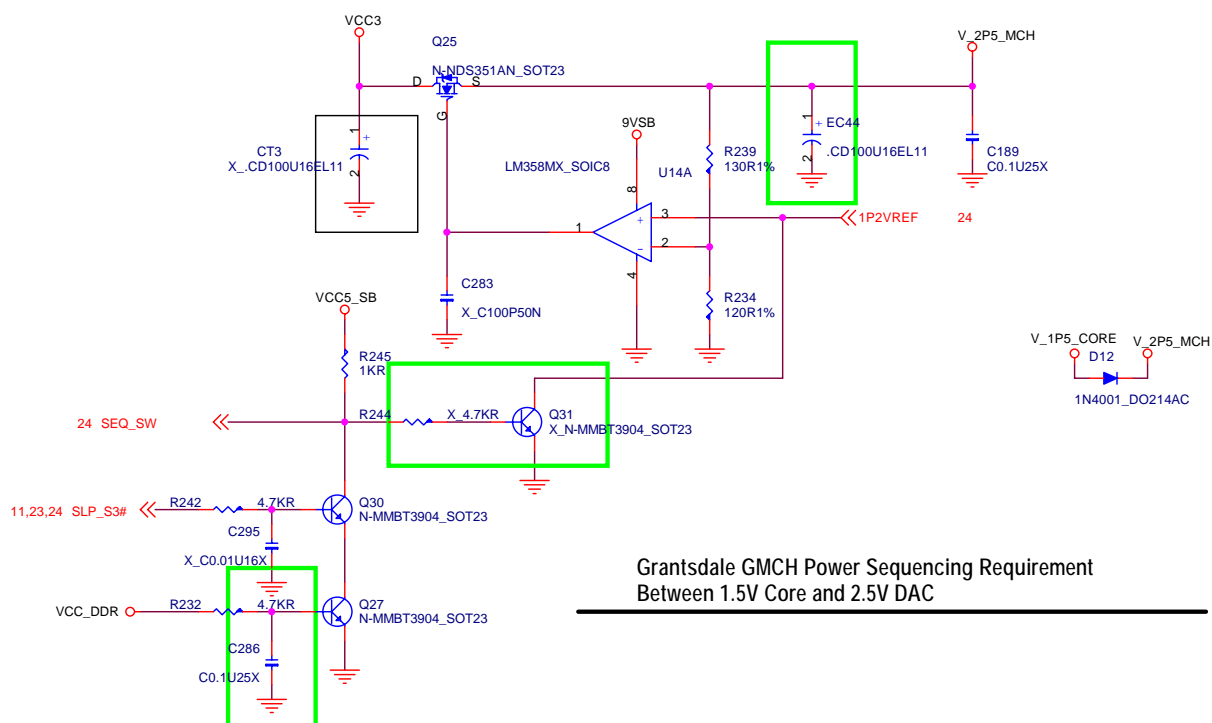
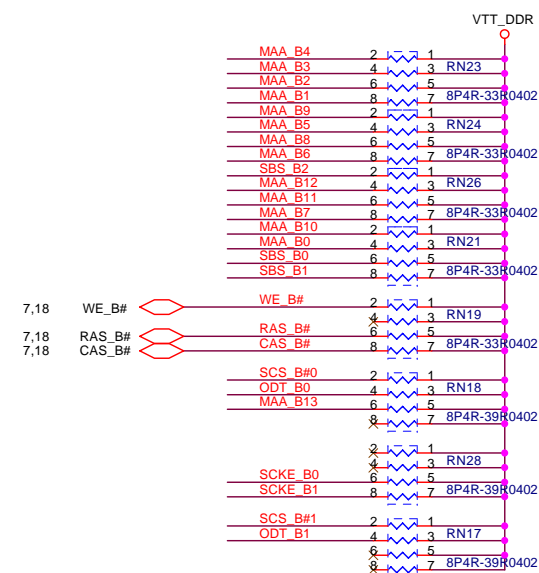
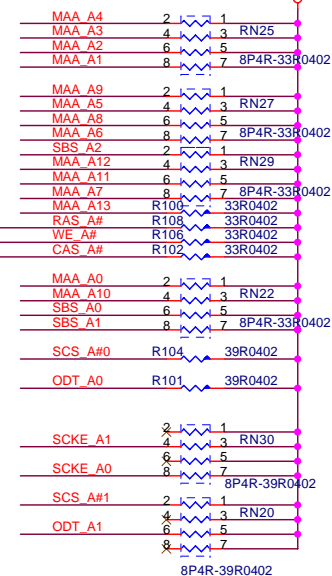
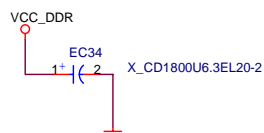
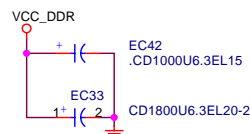
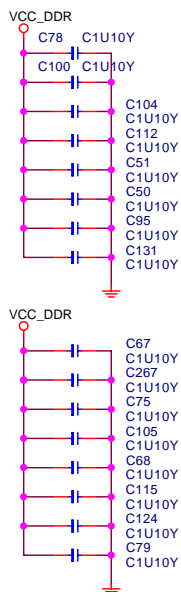
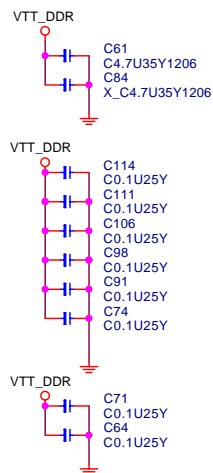


Closer to SB.

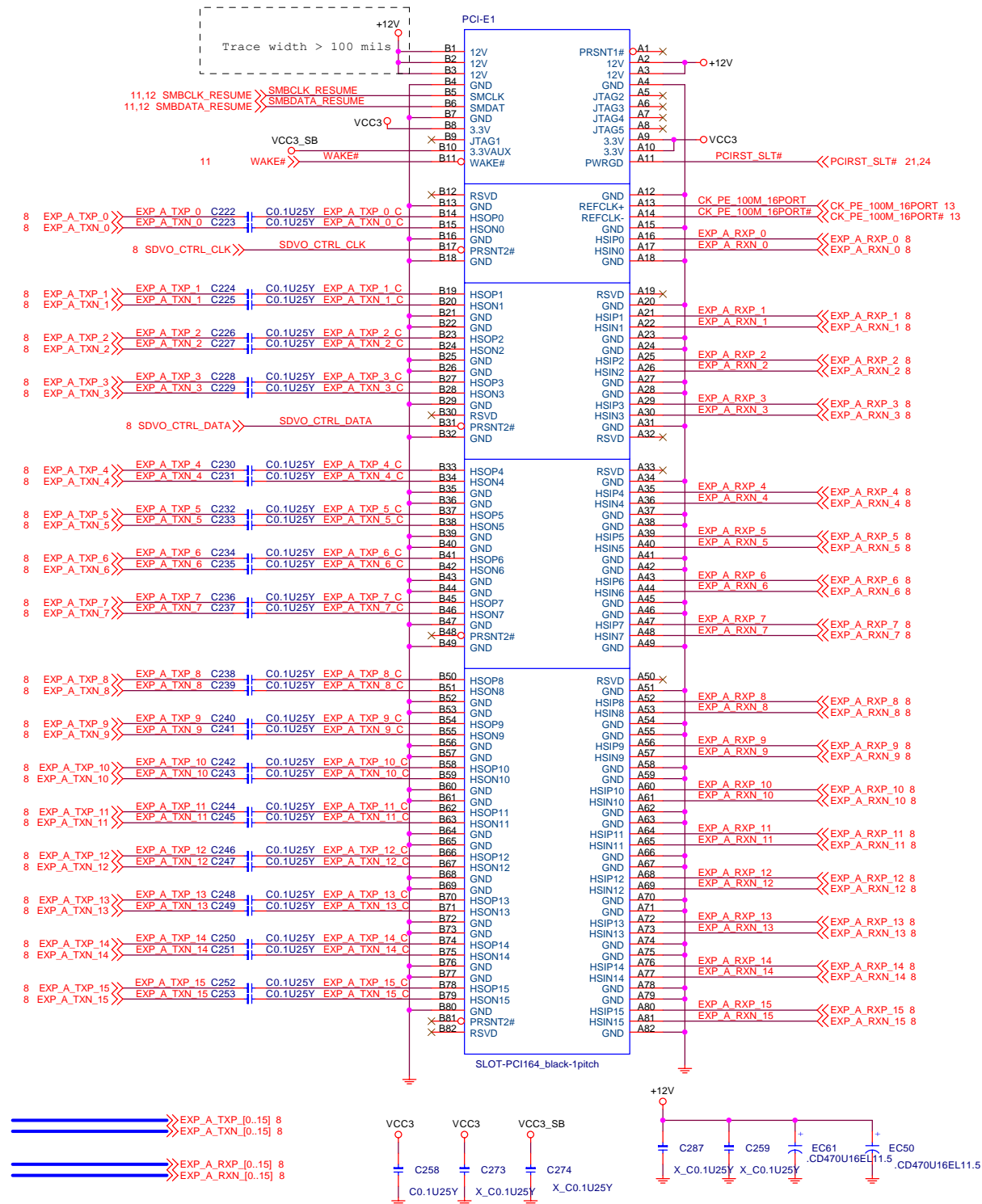
LAN CONNECTOR



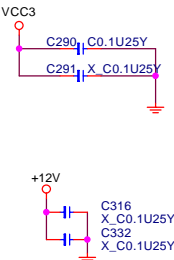




Grantsdale GMCH Power Sequencing Requirement Between 1.5V Core and 2.5V DAC

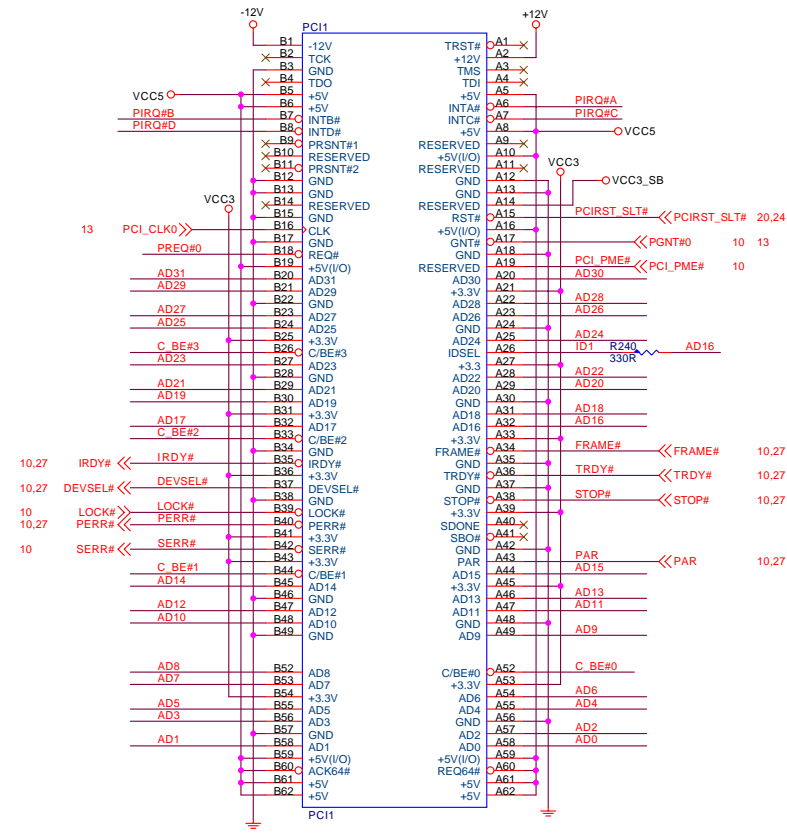


PCI EXPRESS 1-PORT

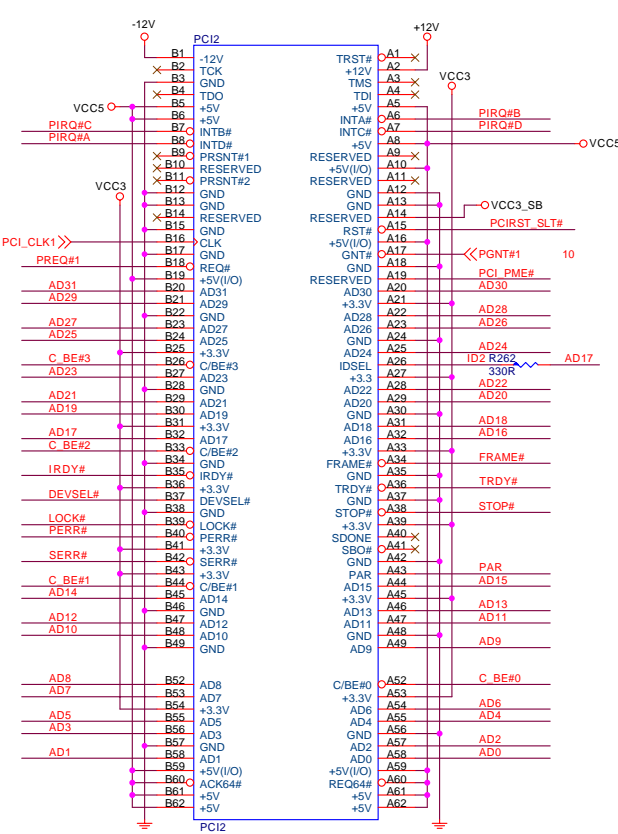


PCI SLOT 1 (PCI VER: 2.2 COMPLY)

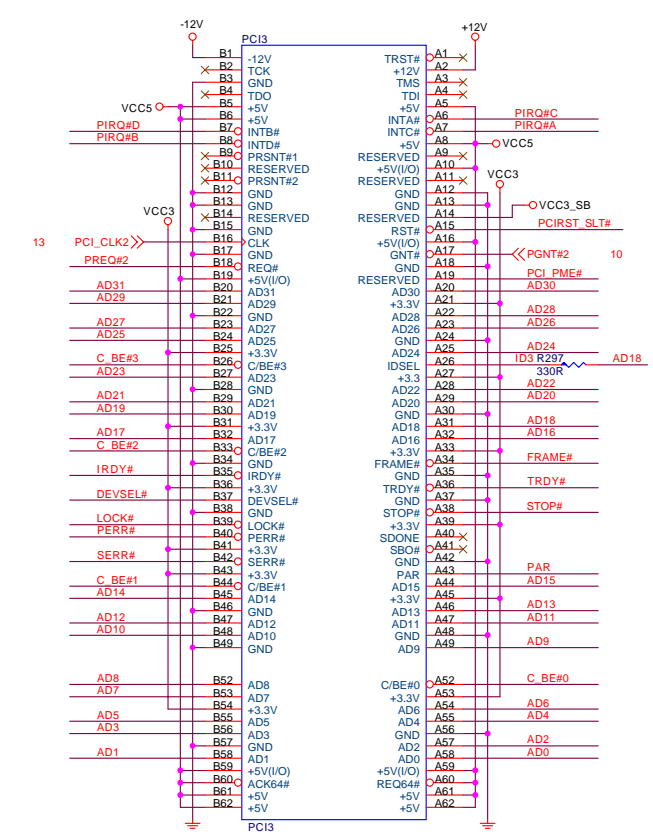
PCI SLOT 2 (PCI VER: 2.2 COMPLY)



ISDEL = AD16
MASTER = PREQ#0
PIRQ#A

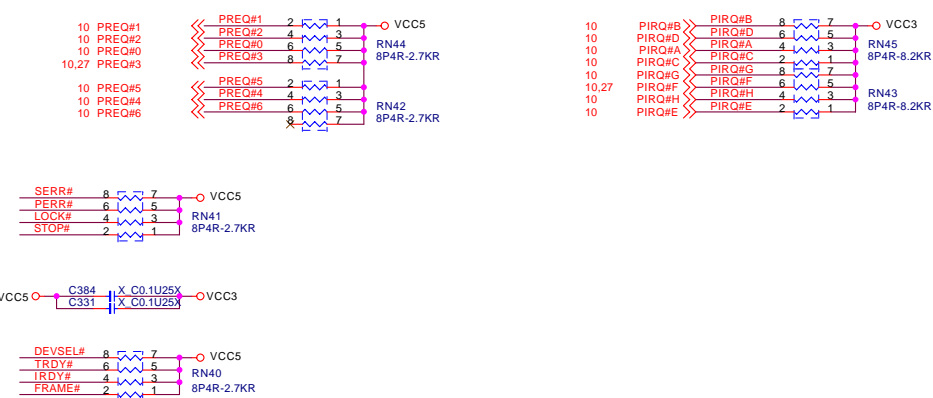


ISDEL = AD17
MASTER = PREQ#1
PIRQ#B

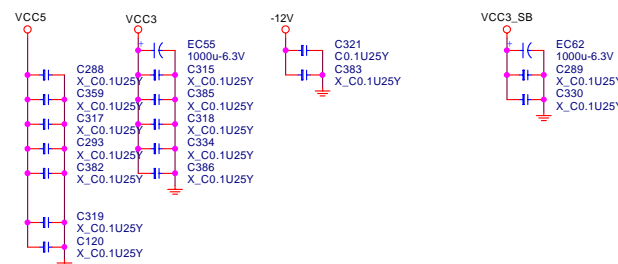


ISDEL = AD18
MASTER = PREQ#2
PIRQ#C

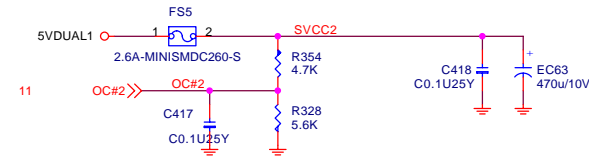
PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS

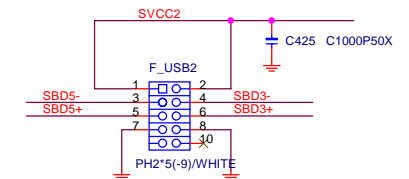


POWER CIRCUIT FOR USB PORT 4,5,6,7 (FRONT)

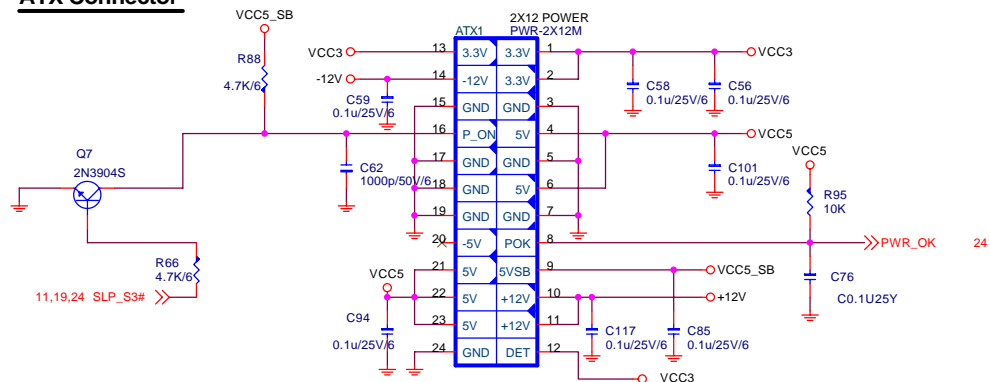


Three schematic diagrams illustrating decoupling capacitor placement:

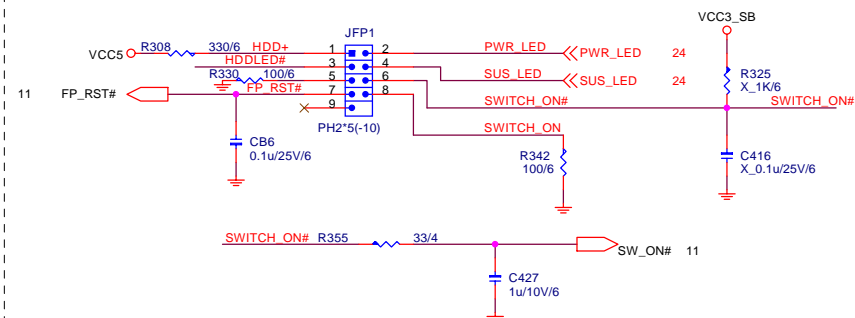
- Diagram 1:** A capacitor labeled **C438** with value **0.1u/25V/6** is connected between **VCC5** and ground. The note below is "Close to C417."
- Diagram 2:** A capacitor labeled **C439** with value **0.1u/25V/6** is connected between **VCC5** and ground. The note below is "Close to C428."
- Diagram 3:** A capacitor labeled **C440** with value **0.1u/25V/6** is connected between **VCC3** and ground. The note below is "Close to R269."



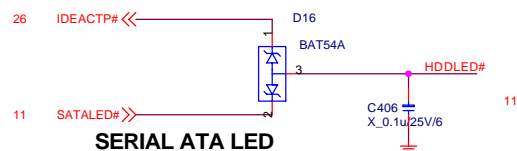
ATX Connector



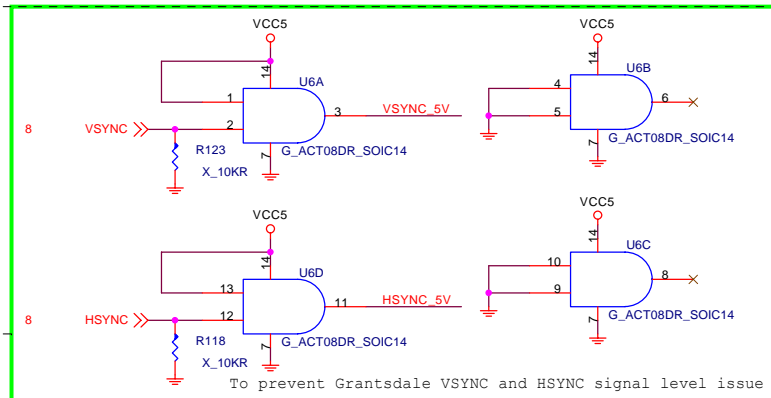
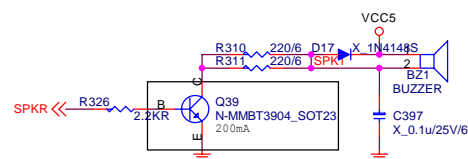
Intel Front Panel



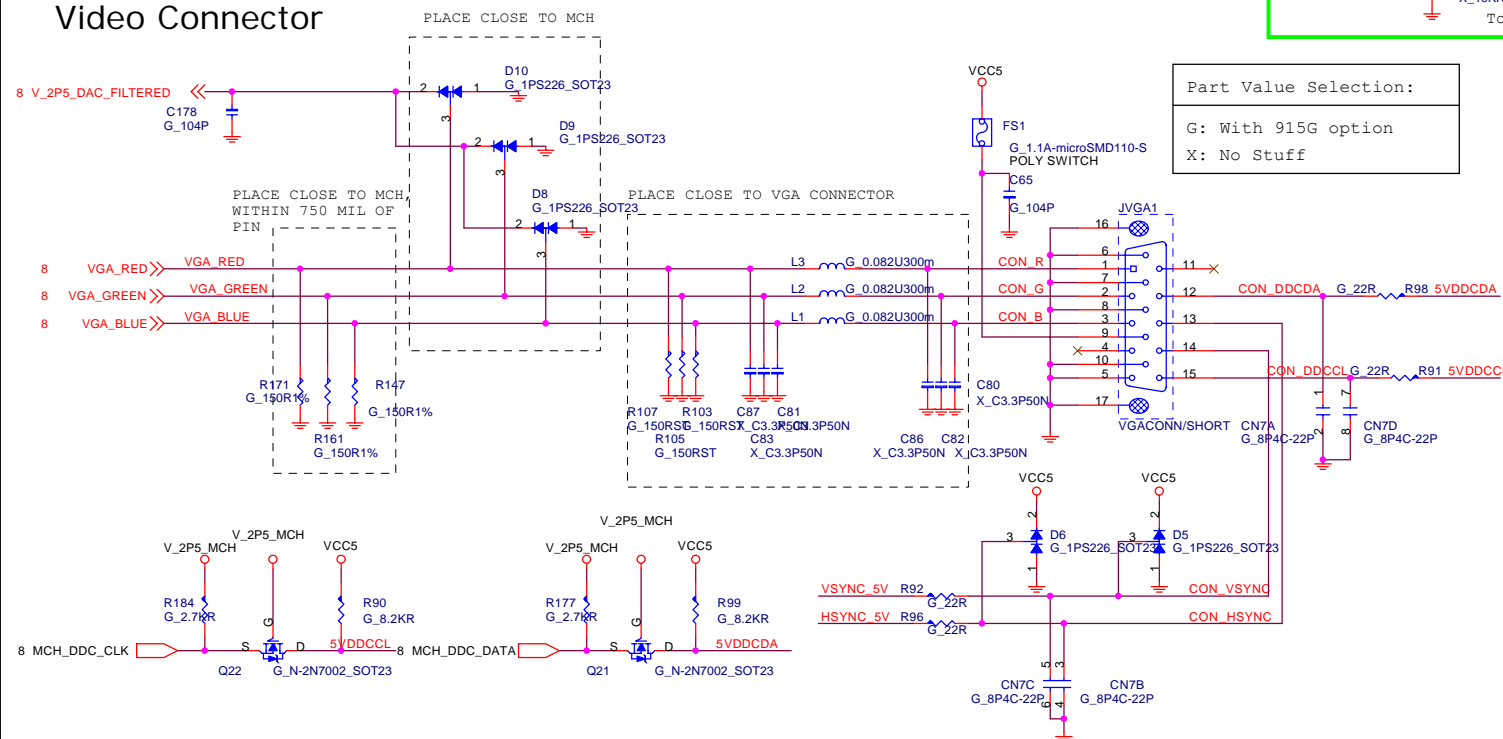
IDE LED



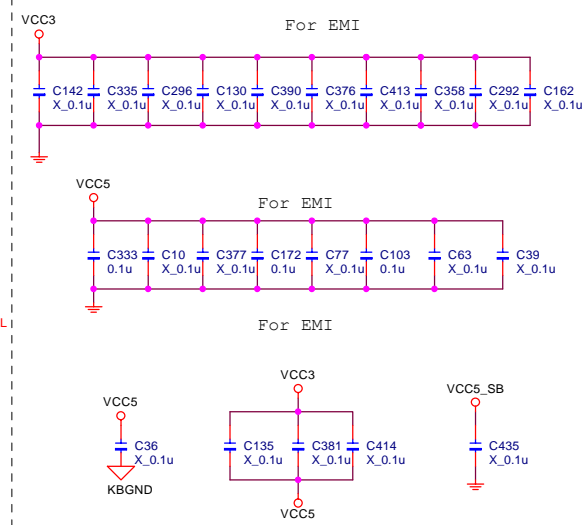
BUZZER



Video Connector



Part Value Selection:
G: With 915G option
X: No Stuff



ACPI Controller

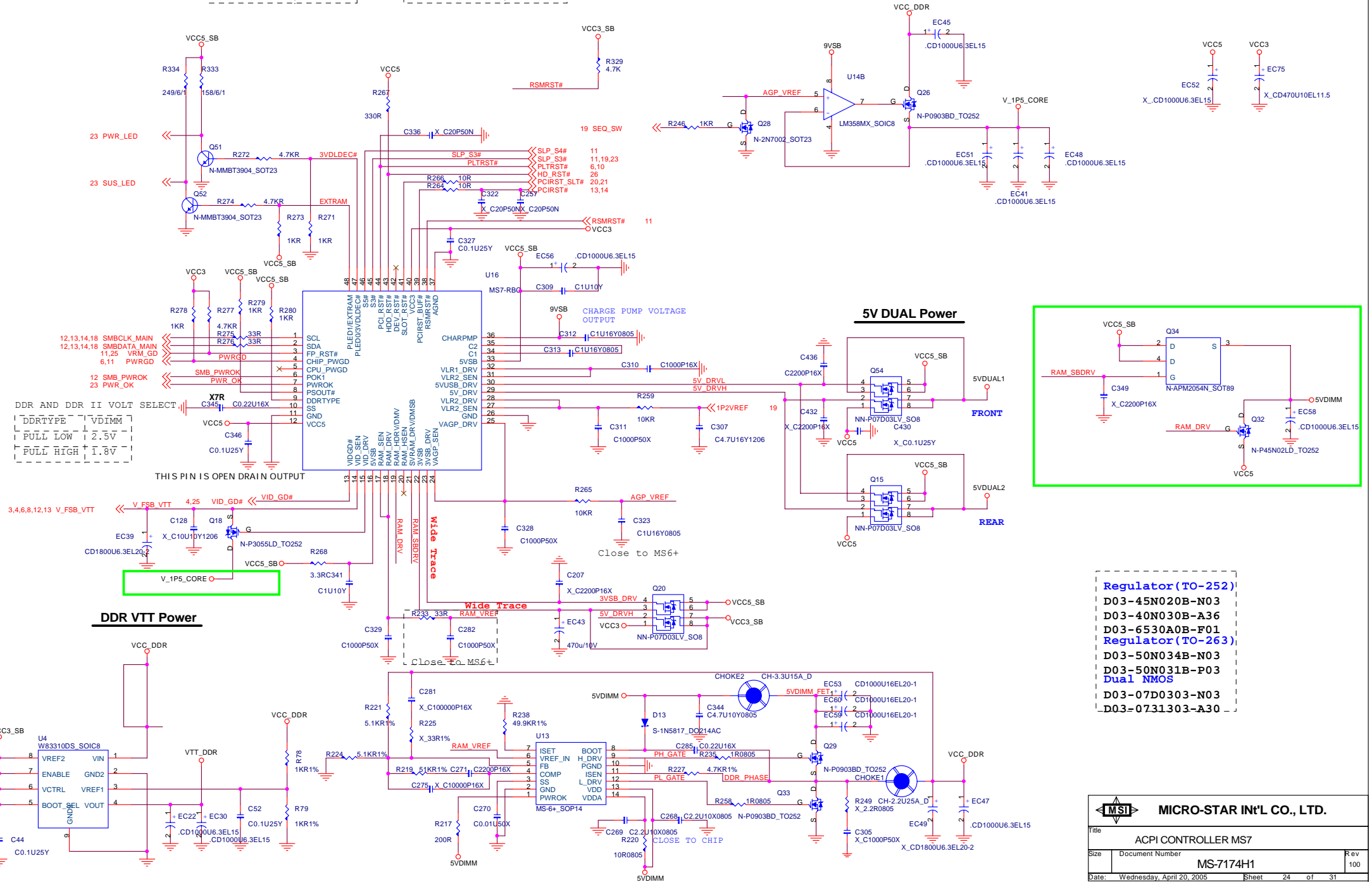
3VSB MODE SELECT

3VSB MODE	3VBLDEC#
SINGLE MOSFET	FULL HIGH
DUAL MOSFET	FULL LOW

VDIMM LINEAR OR PWM SELECT

VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
PWM REGULATOR	PULL HIGH

PCI-Express POWER



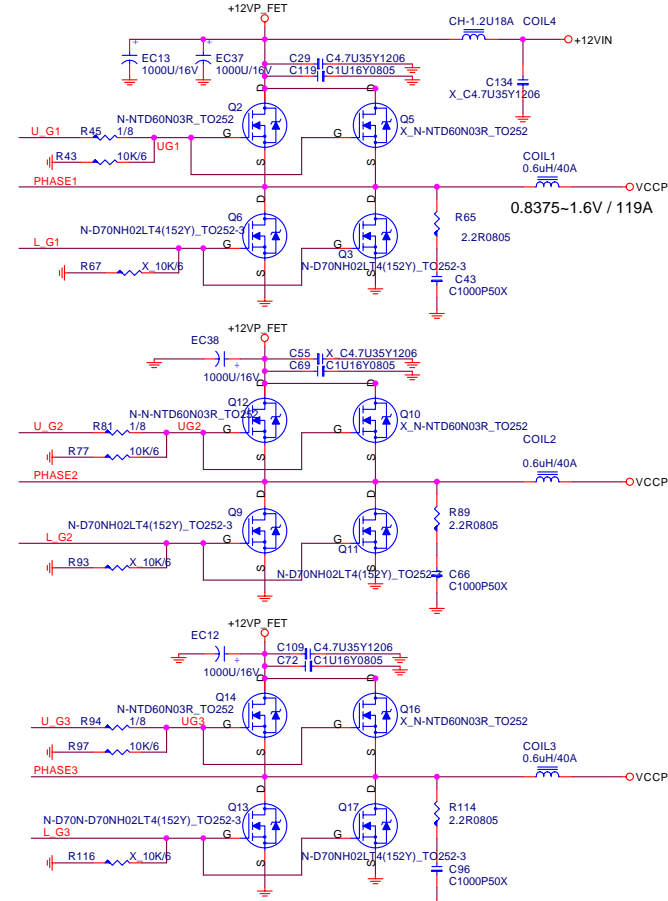
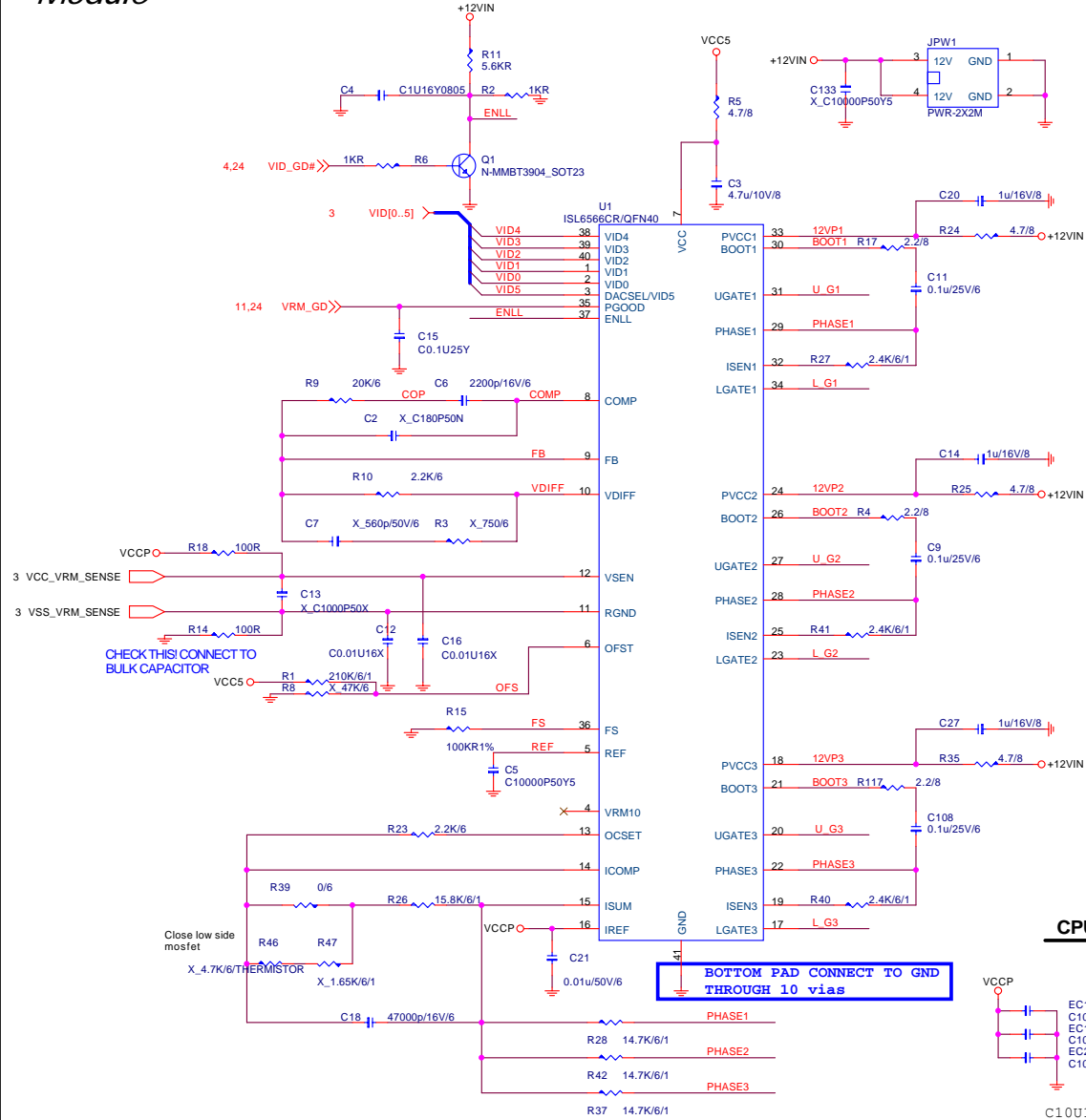
Regulator (TO-252)

D03-45N020B-N03
D03-40N030B-A36
D03-6530A0B-F01
Regulator (TO-263)
D03-50N034B-N03
D03-50N031B-P03
Dual NMOS
D03-07D0303-N03
D03-0731303-A30

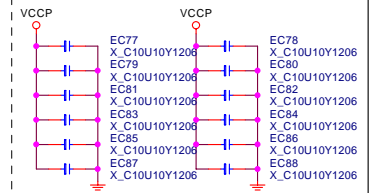
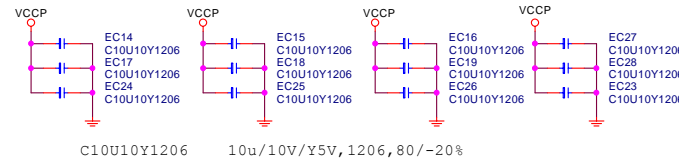
Voltage Regular Module

IPF06N03LA Rds(on)=8.7mΩ(@4.5V,30A), Vgs(on)=1.2~2V, Id=50A, Ciss=3110pf, Qg=10nC, Vds=25V, Vgs=±20V
C100U2SP ESR<13mΩ, Ripple cur.<2.7A, Lc<12uA, 105C
.CD3300U6.3EL25 ESR<12mΩ, Ripplecur.<2800mA, 105C, longlife3000hrs, KZGSeries
560u_2.5V ESR=6mΩ, Ripplecur.=4400mA, Lc.<500uA, 105C/2000hrs
1800UF/6.3V ESR<12mΩ, Ripplecur.<2350mA, 105C, longlife change from 2000hrs to 3000hrs ,KZJ series
0.6uH/40A ESR<12mΩ, Dip-2/vertical17.5mm, 1.2ψ/5.5turns, 18A
CH-1.2U18A

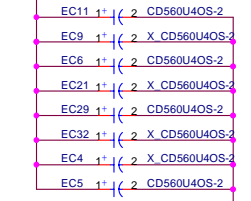
TDP = 115 W
VR_TDC = 101 A
Icc(max) = 119 A
Tejas Tcase = [P x 0.213] + 43.3
Prescott Tcase = [P x 0.25] + 43.3



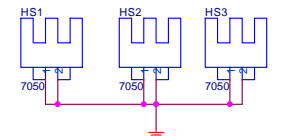
CPU DECOUPLING CAPACITORS



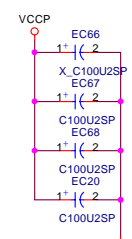
OS-CON Capacitors



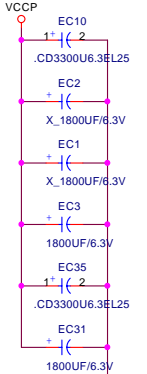
MOSFET Heatsinks



SP Capacitors



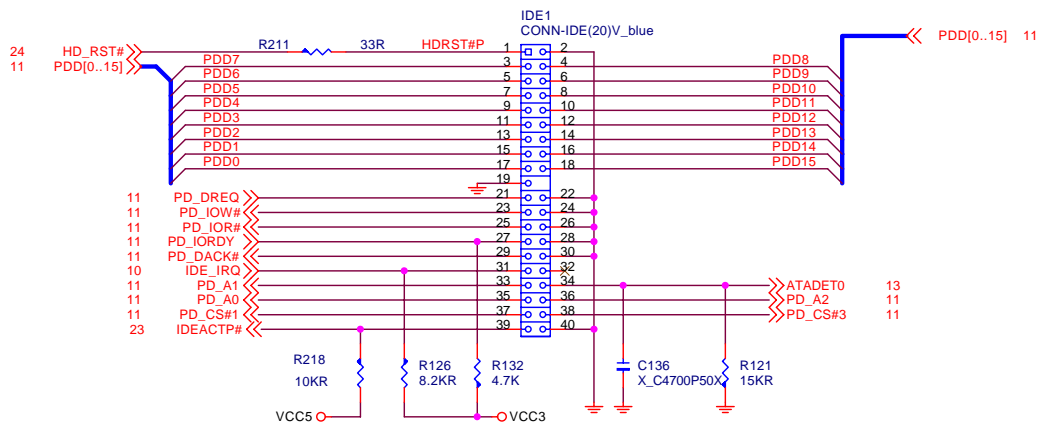
EL Capacitors



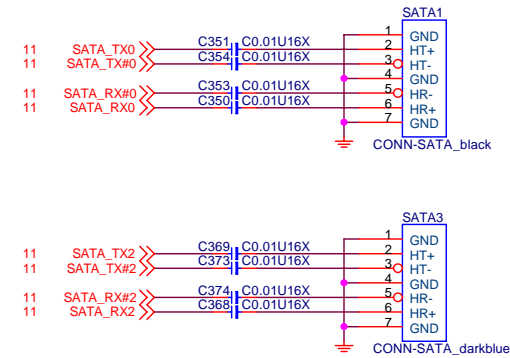
Solder Side

Title VRM 10.1 - Intersil 6565ACV 3 Phase			
Size	Document Number	MS-7174H1	
Date: Wednesday, April 20, 2005	Sheet	25	of 31

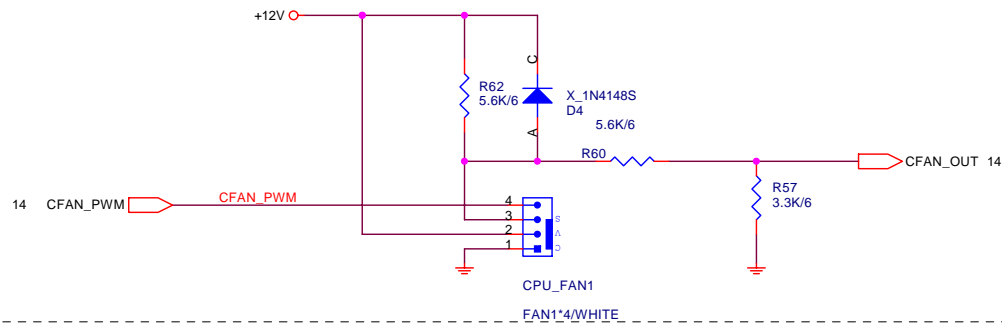
ATA 33/66/100 IDE Connectors



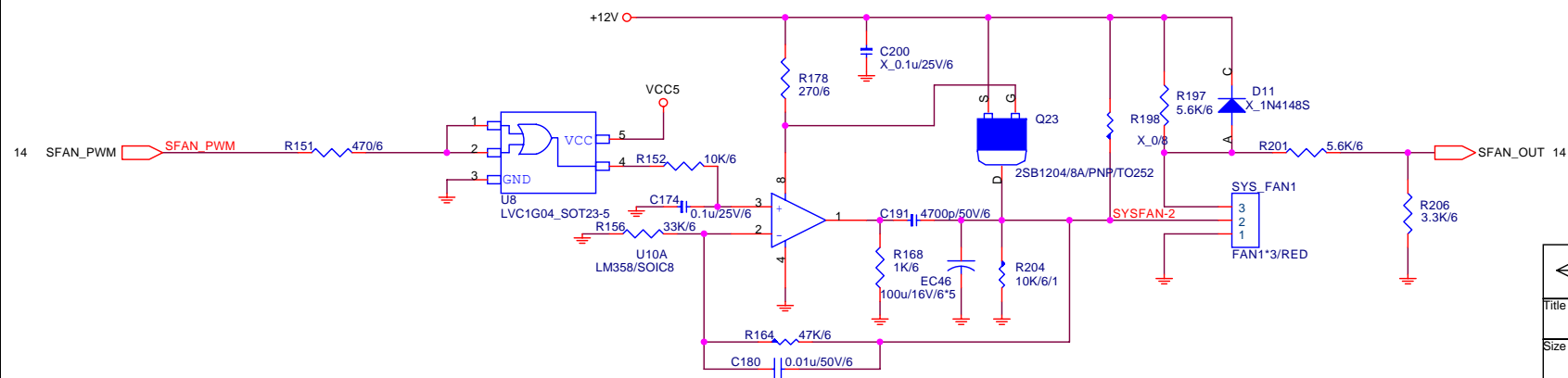
SERIAL ATA CONNECTOR BLOCK



CPU FAN



SYSTEM FAN



MICRO-STAR INT'L CO., LTD.

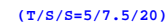
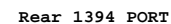
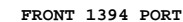
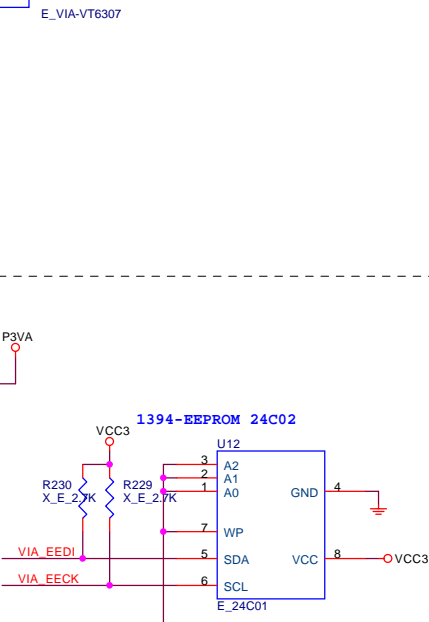
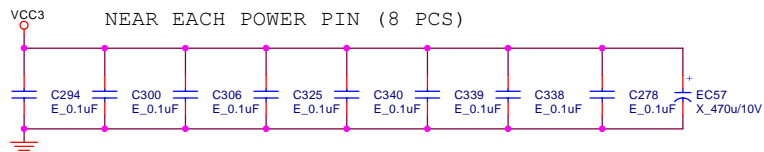
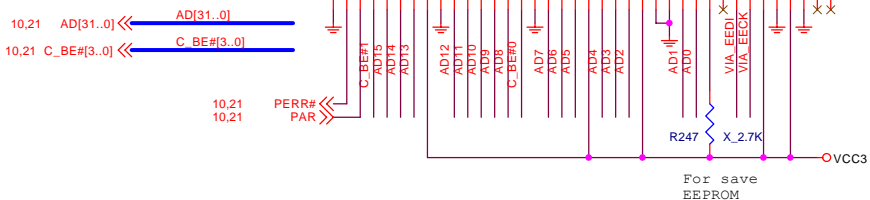
Title			
FAN & IDE Connectors			
Size	Document Number		Rev
	MS-7174H1		100
Date:	Wednesday, April 20, 2005	Sheet	26 of 31

X: No Stuff


```

IDSEL = AD25
MASTER = PREQ#3
PIRQ#F

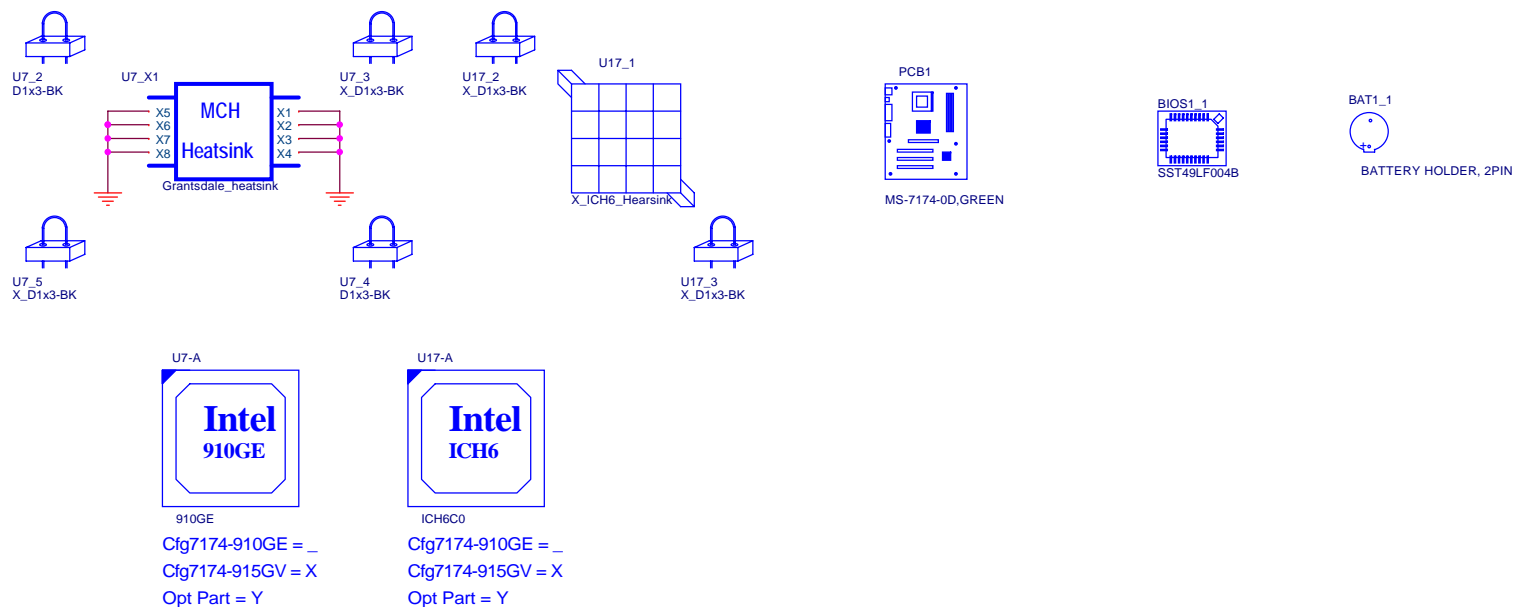
```



Place close to pin 74
(Less then 500 mils)

 MICRO-START INT'L CO., LTD.			
Title			
VIA-6307 IEEE1394 Controller			
Size	Document Number		Rev
A3	MS-7174H1		100
Date:	Wednesday, April 20, 2005	Sheet	27 of 31

MANUAL PART



Model option table

Model type	Function	BOM Config	ERP BOM No.
MS7174	915GV+ICH6+47M997+82562GT+ALC880+3PCI+u-ATX +2PS2+8USB+1COM+VGA+1Audio+LPT+RJ45+Intel pinhead+1394	Cfg7174-915GV	601-7174-***
MS7174	910GE+ICH6+47M997+82562GT+ALC880+3PCI+PCIE X16+u-ATX+2PS2+8USB+1COM+VGA+1Audio+LPT+RJ45+Intel pinhead+1394	Cfg7174-910GE	601-7174-B10